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(71) Applicant:
TEXAS INSTRUMENTS INCORPORATED
Dallas Texas 75265 (US)

(72) Inventors:
- **Olsen, Leif C.**
  Plano, Texas 75025 (US)
- **Swanson, Leland S.**
  Mc Kinney, Texas 75070 (US)
- **Edwards, Henry L.**
  Garland, Texas 75044 (US)

(74) Representative:
Harris, Ian Richard et al
D. Young & Co.,
21 New Fetter Lane
London EC4A 1DA (GB)

(54) Chemical mechanical polishing for isolation dielectric planarization

(57) A fabrication method for an integrated circuit structure, comprising the steps of: forming an oxide structure which includes, distributed there-through, a first layer comprising silicon and carbon; and polishing said oxide structure, using a slurry composition which has a selectivity to said first layer of greater than 10 to 1, so that said polishing step smoothly removes said oxide on a first side of said first layer and stops on exposed areas of said first layer; whereby said exposed areas of said first layer define a uniform surface level for said oxide structure. In an embodiment, silicon carbide is used for a hardmask for the isolation dielectric etch and also serves as an etch stop for chemical-mechanical polishing. Alternatively, silicon carbonitride or silicon carboxide can be used.

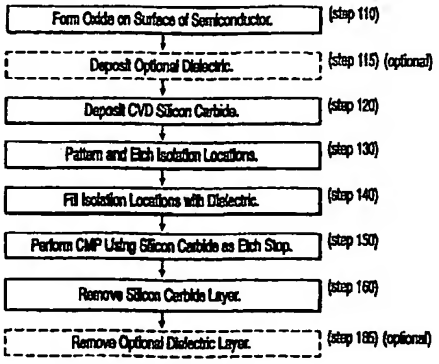

FIG. 1

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EUROPEAN SEARCH REPORT

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 5 362 669 A (BOYD JOHN M ET AL) 8 November 1994 (1994-11-08)	1-6,8,9	H01L21/3105
A	* column 3; figures 1-3 *	7	
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TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19 October 1999	Szarowski, A

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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